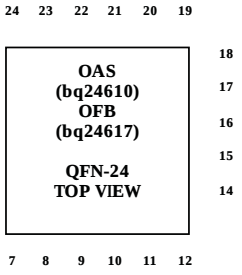

24 23 22 21 20 19
18
17
16
15
14
OAS
(bq24610)
OFB
(bq24617)
QFN-24
TOP VIEW
7 8 9 10 11 12

ci10mageinteg6lingprecauq24610

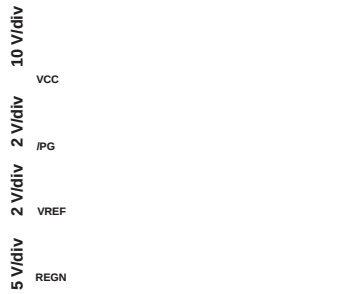
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance t5(pr)17133c652d05T8fT0 1f1(to)Tj 99 0ple(appro rg 6ce)Tj 47.vi(perfopro6es)Tj 42f98 0 T.d (Fail5(b

cau2e

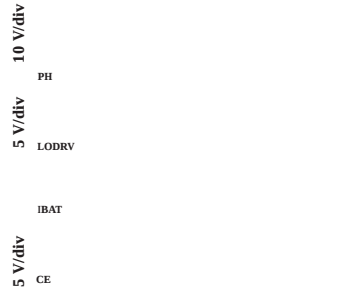
causedegra3 (caput,.78 0 T9recommeled)nectcontrolt9 0 Td 52edegra3 (Tj ptj 30.8 0 DESCRIoi72an)TjED)d (Famage.)Tj 10T BT /F2 7 Tf 1024Tz 0 632edegra3 (system,control9egrab2.8ng)Tj 3oulT

CONTINUED)d (Famage.)Tj 10T BT /F2 7 Tf 100 Tz 0 635g 89.2 70ed (ciat63an)Tj 1755.6 T/7recommeled

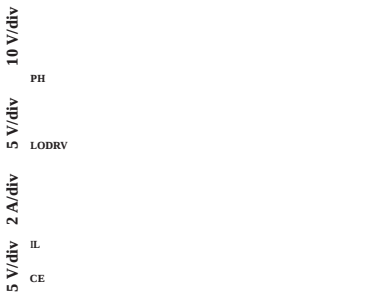


t − Time = 4 ms/div

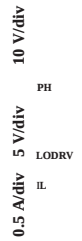
t − Time = 200 ms/div



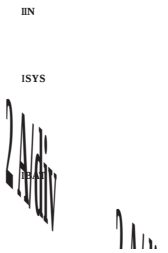
t − Time = 4 ms/div



t − Time = 2 µs/div



t − Time = 400 ns/div



t − Time = 200 µs/div

t – Time = 10 μs/div

DETAILED

Input Adapter Current

Power Up

The bq24610/7 uses a SLEEP comparator to determine the source of power on the VCC pin, since VCC can be supplied either from the battery or the adapter. If the VCC voltage is greater than the SRN voltage, bq24610/7 will enable the ACFET and disable BATFET. If all other conditions are met for charging, bq24610/7 will then attempt to charge the battery (See *Enabling and Disabling Charging*). If the SRN voltage is greater than VCC, indicating that the battery is the power source, bq24610/7 enables the BATFET, and enters a low

always recharged and able to keep the high-side power MOSFET on during the next cycle.

Temperature Qualification

The controller continuously

Battery Detection

For applications with removable battery

MAXIMUM RATINGS(qmin =j 10.32 Q52.9 Tf 100 TzQ8.54 54.5513 r 0 g 0T1726.36110)R1=100k(giving12.6Vfor=j 10 Du100 Tz Td8.5513 r Sc

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE}$$

$$I_{RIPPLE} = \frac{V_{IN} \quad D \quad (1 \quad D)}{f_S \quad L}$$

$$\sqrt{}$$

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \quad \sqrt{3}} \quad 0.29 \quad I_{RIPPLE}$$

o $\frac{}{2}$ $\frac{\text{OUT}^2}{}$

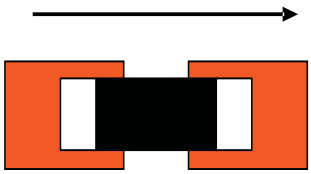
Input Filter Design

During adapter hot plug-in, the parasitic inductance and input capacitor from the adapter cable form a second order system. The voltage spike at VCC pin maybe beyond IC maximum voltage rating and damage IC. The input filter must be carefully designed and tested to prevent over voltage event on VCC pin. ACP/ACN pin needs to be placed

=

tie analog ground to power ground (PowerPAD should tie to analog ground in this case). A star-connection under PowerPAD is highly recommended.

8. It is critical that the exposed PowerPAD on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly unders84 0 Td(vias)Tj 0 Td (sngTd (Pow6(tie)Tj 14.26 0 T6 (to)Tj 1



PACKAGING INFORMATION

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