- **Four Analog Inputs, Four BTL Power Outputs**
- **Typical Output Power at 10% THD+N**
  - **28 W/Ch Into 4 Ω at 14.4 V**
  - **50 W/Ch Into 2 Ω at 14.4 V**
  - **79 W/Ch Into 4 Ω at 24 V Patented Pop- and Click-Reduction Technology**
  - **Soft Muting With Gain Ramp Control**
  - **Common-Mode Ramping**

Heat Slug Up for the TAS5424B-Q1

- **44-Pin PSOP3 (DKE) Low-Standoff Power SOP Package With Heat Slug Up for the TAS5424B-Q1**
- **64-Pin QFP (PHD) Power Package With Heat**

APPLICATIONS

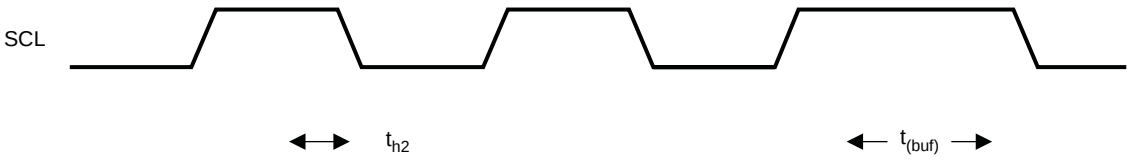
- **OEM/Retail Head Units and Amplifier Modules Where Feature Densities and**

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

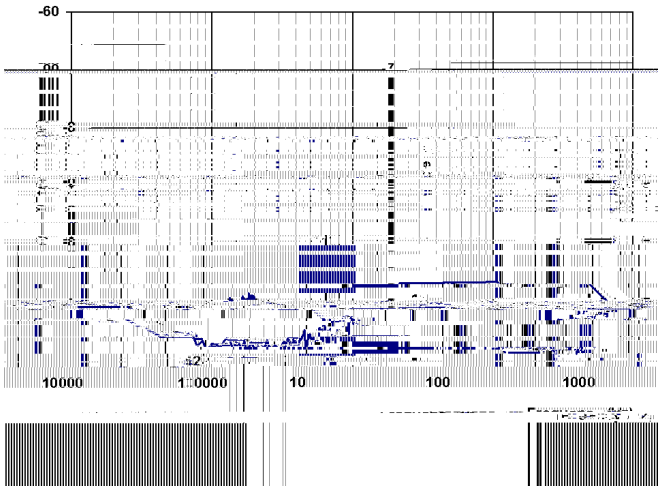
FUNCTIONAL BLOCK DIAGRAM

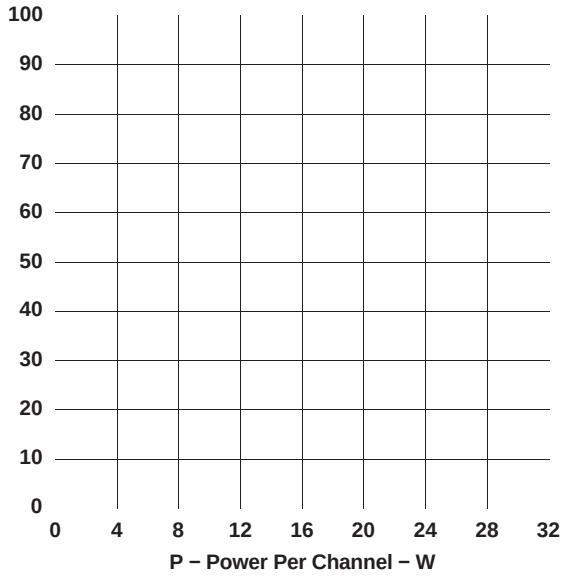
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
19 20

SCL



SDA


-60
10000
1 0000
10
100
1000


100
90
80
70
60
50
40
30
20
10
0
0
4
8
12
16
20
24
28
32
P − Power Per Channel − W

DESCRIPTION OF OPERATION

The user may restart the affected channel via I^2C. An OCSD event activates the fault pin, and the affected channel(s) are recorded in the I^2C fault register. If the supply or ground short is strong enough

I²C Serial Communication Bus

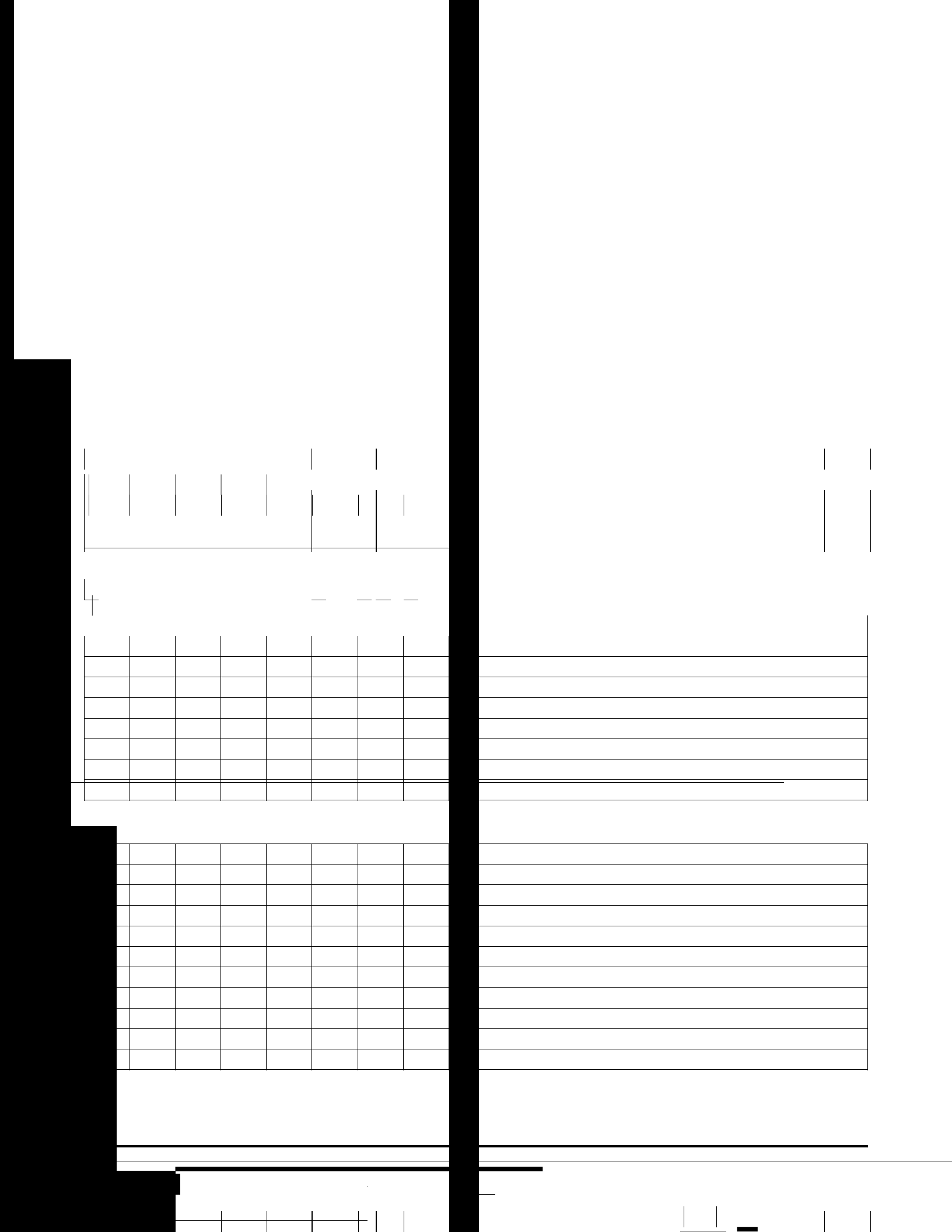
The device communicates with the system processor via the I²C serial communication bus as an I²C slave-only device. The processor can poll the device

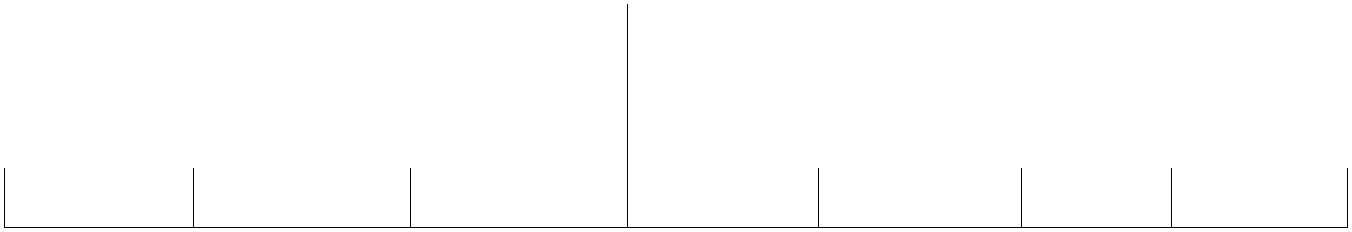
transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the HIGH level for the bus. There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus.

Figure 13. Typical I^2C Sequence

Use the I2C_ADDR pin (pin 2) to program the device for one of four addresses. These four addresses are licensed I^2C addresses and do not conflict with other licensed I^2C audio devices. To communicate

TAS54168AND the





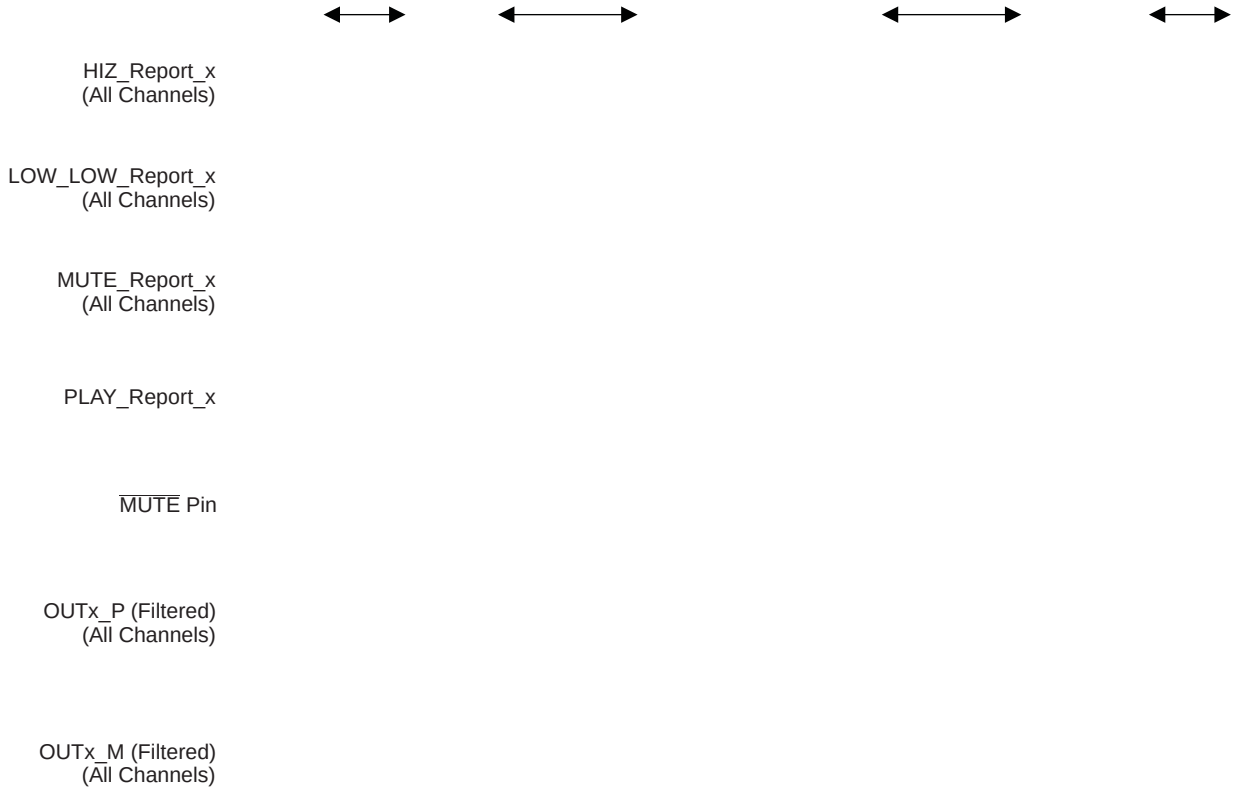


Figure 18. Click- and Pop-Free Shutdown and Restart Sequence Timing Diagram

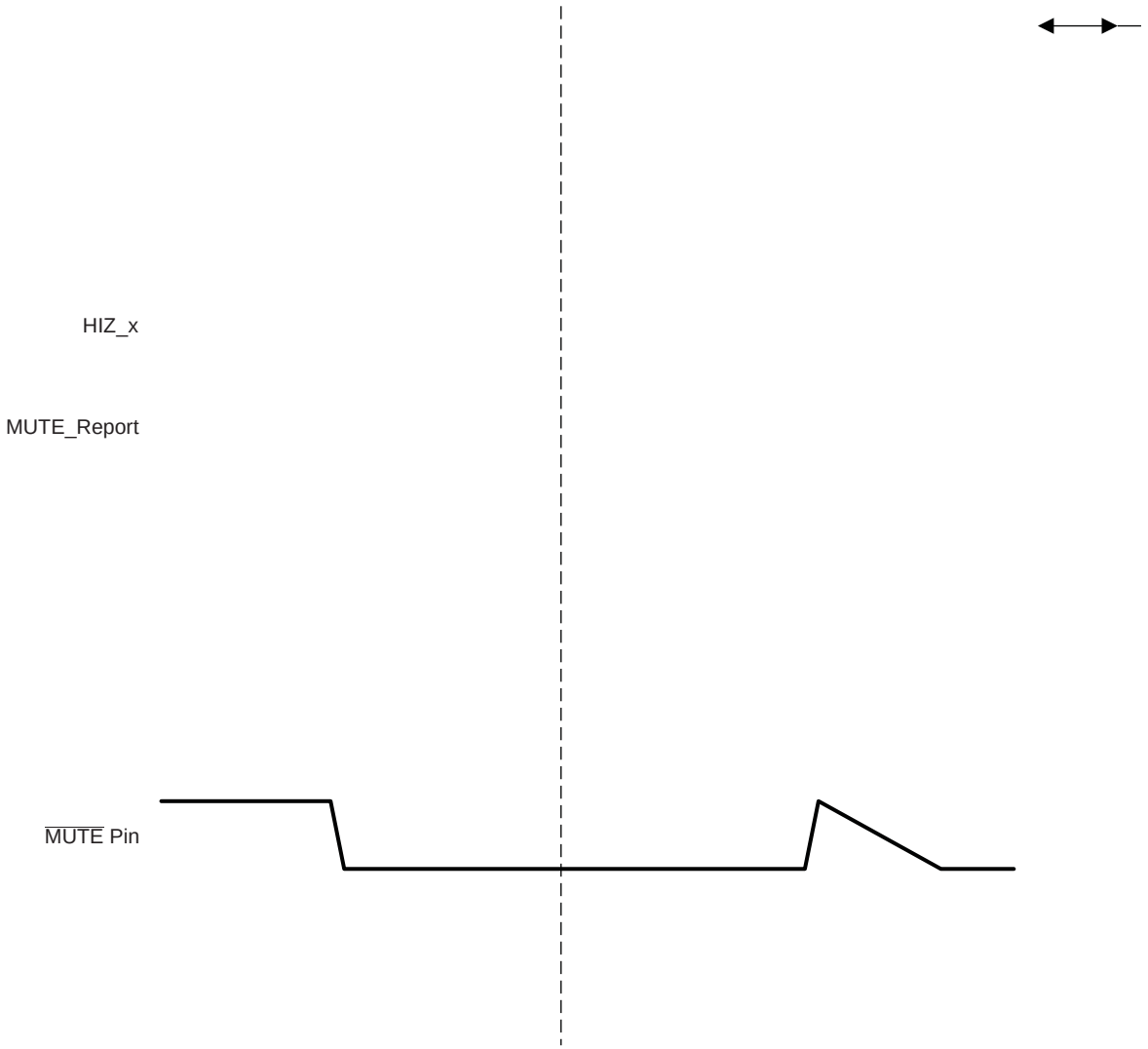
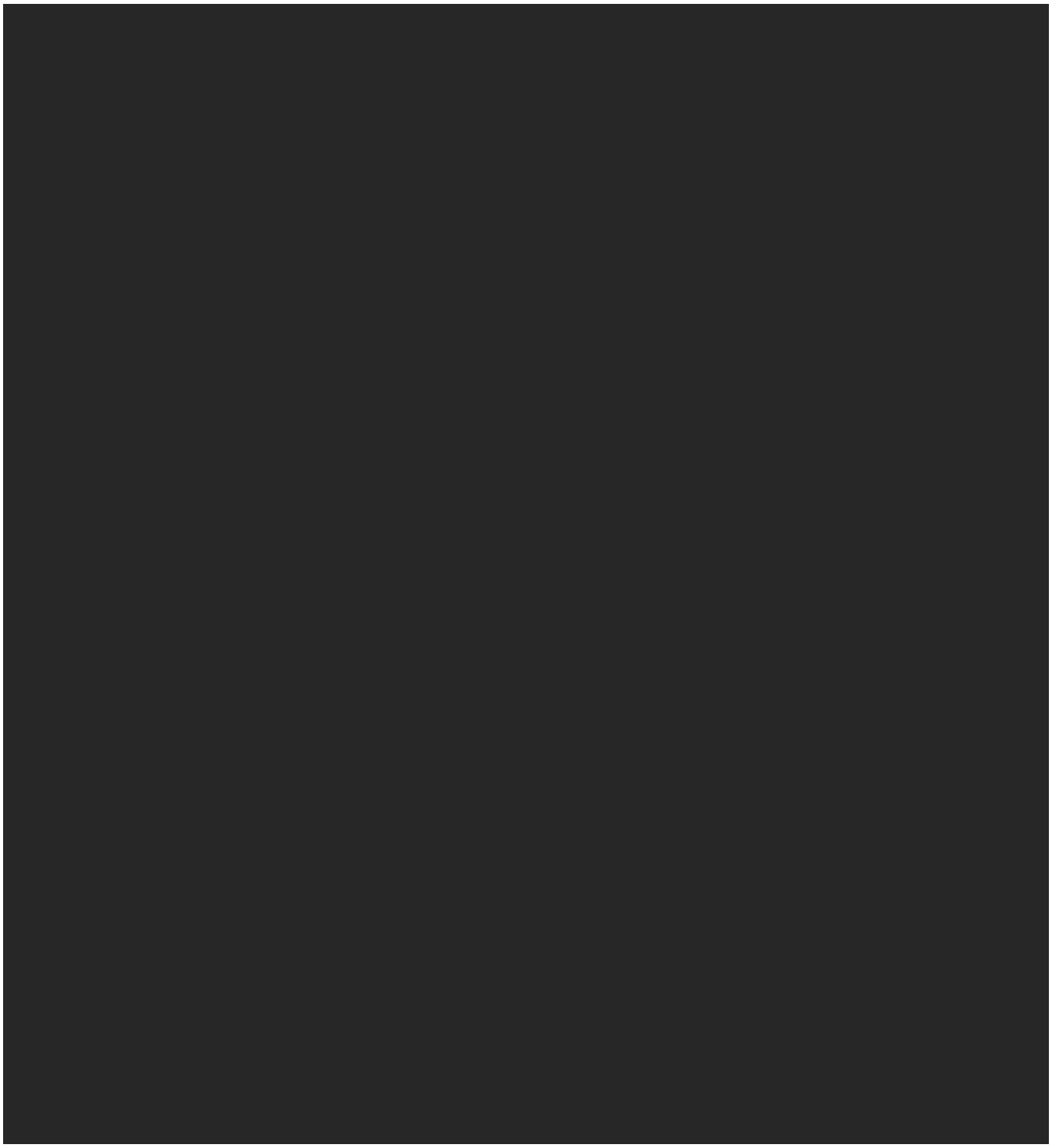

HIZ_x
MUTE_Report
MUTE Pin

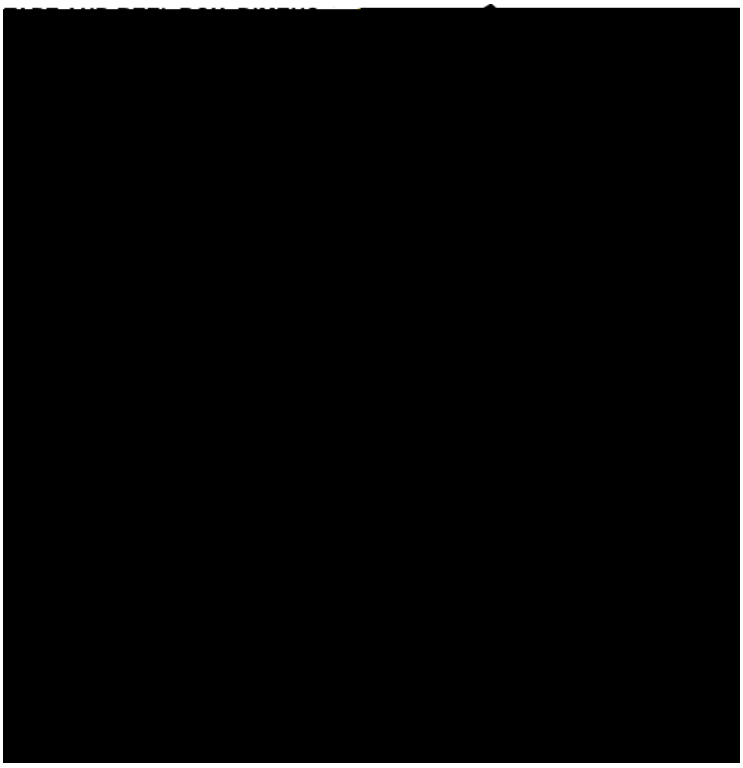
Figure 20. Latched Global Fault Shutdown and Individual Channel Restart Timing Diagram (UV Shutdown and Recovery)



performance and even power dissipation on multiple channels. For smooth power up, power down, and mute operation, the same control commands (such as mute, play, Hi-Z, etc.) should be sent to the paralleled channels at the same time. Load diagnostic is also supported for parallel connection. Paralleling on the device side of the LC output filter is not supported, and can result in device failure due to

TAPE AND REEL INFORMATION

*All dimensions are nominal

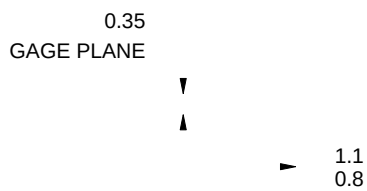


*All dimensions are nominal

Device

PACKAGE OUTLINE

C ◄

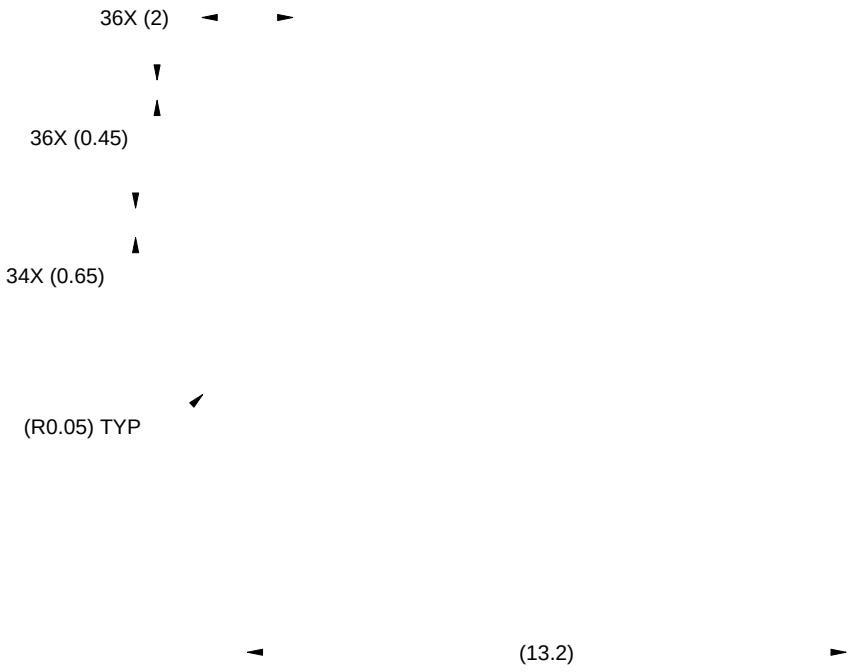


EXAMPLE BOARD LAYOUT

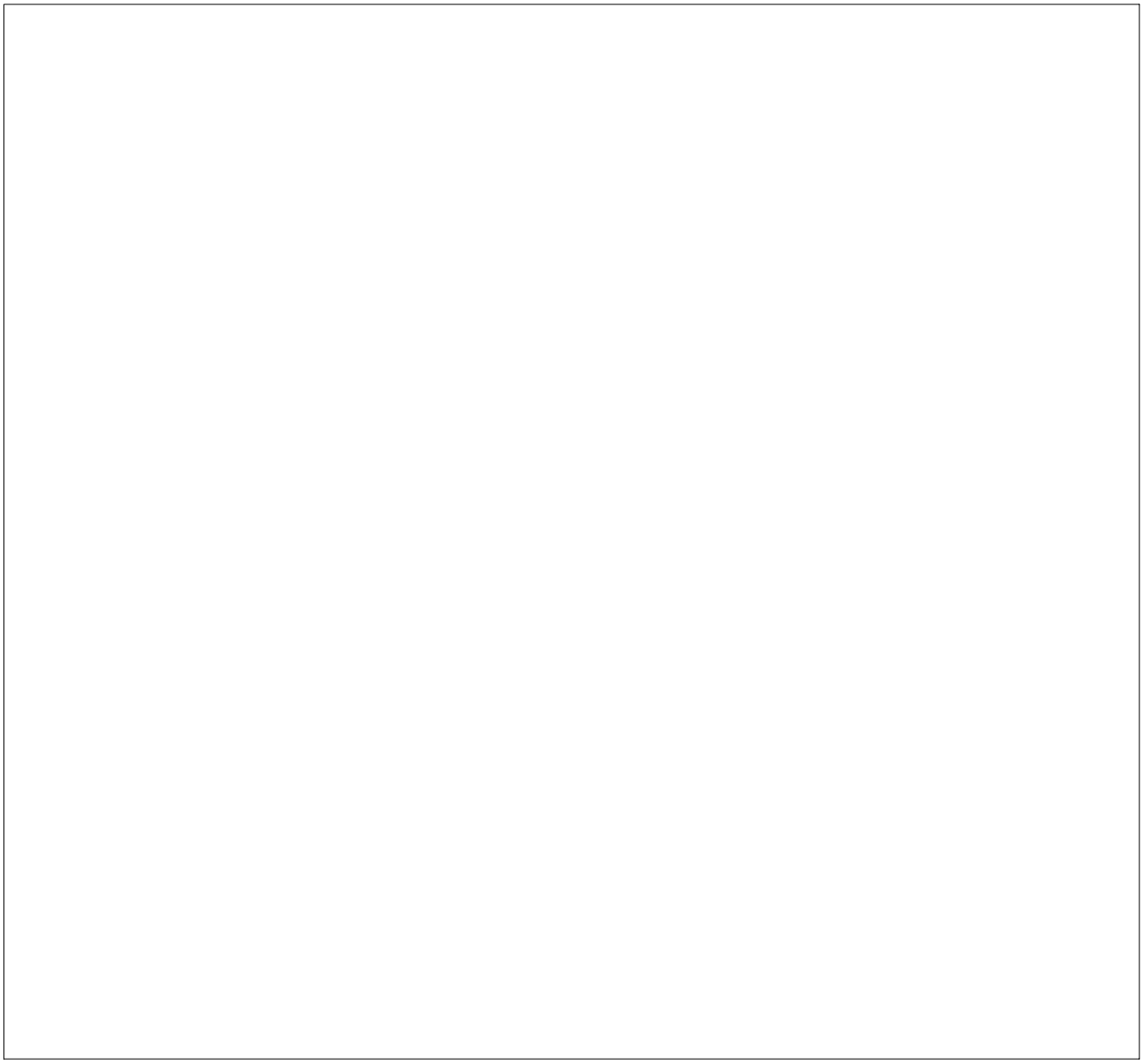
EXAMPLE STENCIL DESIGN

DKD0036A

PowerPAD SSOP - 3.6 mm max height



PowerPAD PLA



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